Planning for Packaging-*Test*-Trim in the High Volume Production of MEMS Devices

21st October 2009

Raj Gupta, PhD
Volant Technologies, Inc.

Outline

- Background.
- Motivation.
- Challenges facing the testing of packaged sensors:
  - During development.
  - In low-to-mid volumes.
  - For high volumes.
- Options available for testing sensors in high volumes.
- Trends in current approaches to testing in high volume.
- Conclusions and strategies going forward.

About Volant Technologies

- Broad and deep business & technical expertise in:
  - Silicon sensors – specifically pressure & acceleration.
  - Sensor integration, and wireless electronics.
  - Materials testing, and finite-element modeling.
- Focus areas:
  - Product & Technology Strategy.
  - Product Execution.
  - Business Development.
  - Foundry Partnering & Prototyping.
  - Cost Reduction, Miniaturization, and Performance Improvement.

Industries Served in 2008

- Application areas:
  - Large-screen optical displays.
  - Construction & security.
  - Alternative energy.
- Select clients:
  - UniPixel Display Corporation, Inc.
  - Lockheed / Savi Technologies, Inc.
  - AccuCrete, Inc.
  - Goldman Sachs.
  - Advanced Energy Capital.
- We serve on the advisory board of 3 start-ups.

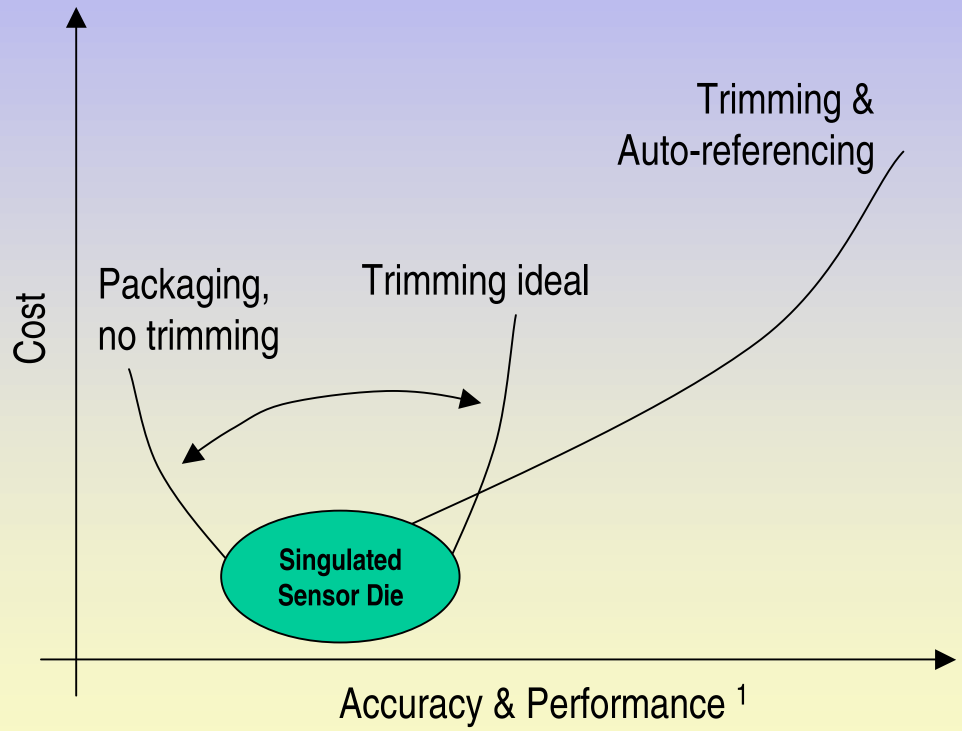
Outline

- Background.
- Motivation.
- Challenges facing the testing of packaged sensors:
  - During development.
  - In low-to-mid volumes.
  - For high volumes.
- Options available for testing sensors in high volumes.
- Trends in current approaches to testing in high volume.
- Conclusions and strategies going forward.

Why is it Package → Test → Trim?

- Sensors sense everything.

  Senturia, "Every MEMS sensor is also a 1st-order strain sensor."



- What makes this different from IC's?
  - Electronics (especially digital) can be easily separated from mechanical effects.
  - Crystal silicon perfected for electronics over more than 75 years.
  - Silicon is only one material among many used by MEMS sensors and actuators.
  - Fully automated solutions for MEMS only now emerging.

[1] Graph adapted from Carver & Looney, "MEMS accelerometer calibration optimizes accuracy for industrial applications", October 27, 2007.

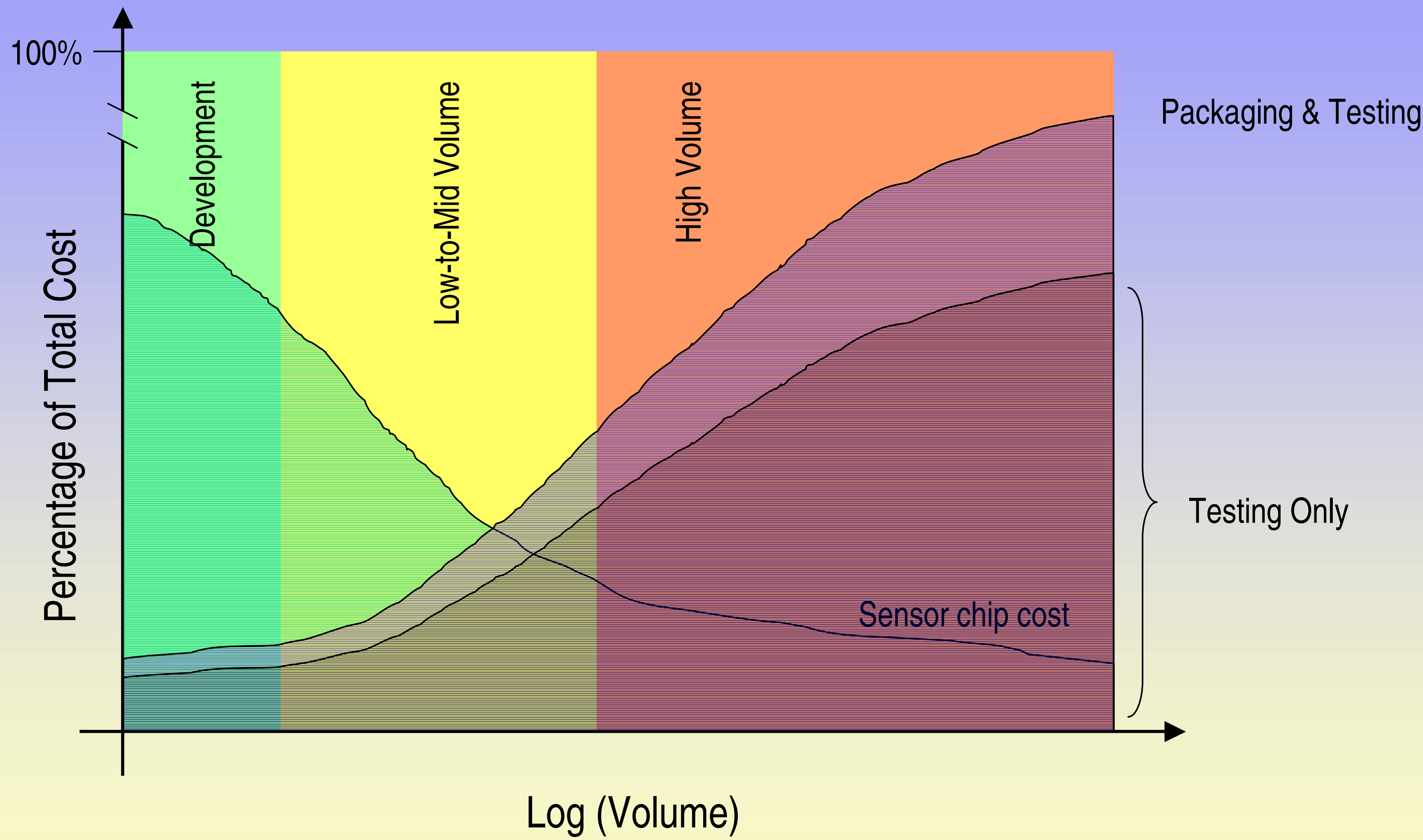
Questions to Ponder

- What can we learn from 50+ years of silicon sensor history?
- How do we break the paradigm of Package → Test → Trim?
  - Is it possible?
- Show me the money…
  - Where should our resources be focused?
- How do choices we make during design, development, and prototyping affect our readiness for manufacturing?

Outline

- Background.
- Motivation.
- Challenges facing the testing of packaged sensors:
  - During development.
  - In low-to-mid volumes.
  - For high volumes.
- Options available for testing sensors in high volumes.
- Trends in current approaches to testing in high volume.
- Conclusions and strategies going forward.

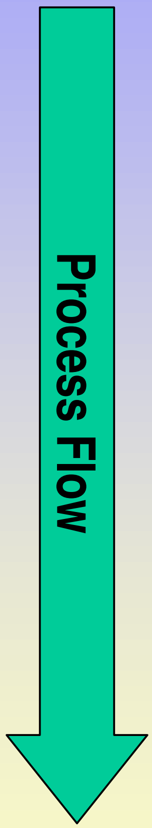
Trends


100%
Development
Low-to-Mid Volume
High Volume
Packaging & Testing
Testing Only
Sensor chip cost
Percentage of Total Cost
Log (Volume)

Types of Tests

- Process:
  - Dopant levels
  - Materials & geometry
- Electrical:
  - Continuity / ESD
  - Burn-in
- Transduction Performance:
  - Sensitivity
  - Calibration
- Mechanical Integrity
  - Physically broken sensor chip
  - Hermiticity / encapsulant
  - Drift / offset / TC's
  - Shock

- Intra-process-level
- Wafer-level
- Die-level
- Packaged-level
- Trimming
- Assembly



Experiences & Observations

- Packaging, test, and performance intimately linked.
- Sufficient variability in process to require testing along the way.
- Many stages of testing and different types of tests called upon.
- Testing becomes progressively more involved and complex further into the process flow and product integration.
- Process flow often not vertically integrated and poor feedback of test data to previous stages.
- Testing affects throughput, and it is often a rate-limiting step.
  - Inherent, intrinsic limitation due to mechanical time-constants.

Development: Process Sensitivity

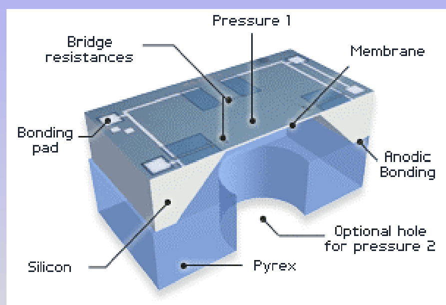
- Difficult to test for overall performance at wafer & die level.
  - Only inferences can be made based on material properties, geometry, and electrical characteristics.
- Industry standard test structures & procedures lacking, because:
  1. processes / run-cards are intensively variable and constitute trade secrets,
  2. there are a range of materials and transducer types, and
  3. material properties are highly process sensitive.

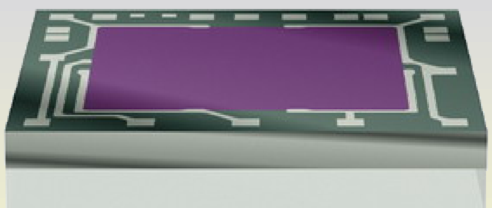
  - This will remain true in low-to-mid volume applications.
  - Standardization possible in high-volume and with fabless approaches.

Low-to-Mid Volume: Customization

Example: piezoresistive pressure sensors

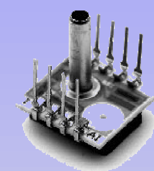
Die



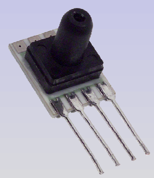


Package Examples

DIP



T0-8



INP

… various others

Applications

Meteorology

Farming

Military

Medical

Automotive

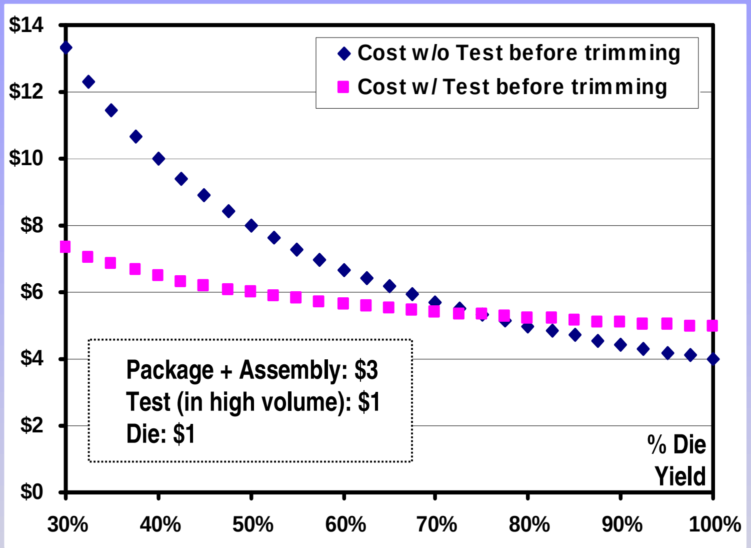
HVAC

… many, many more

Variants may include open or closed bridge, absolute vs. gauge vs. differential

Typically 5 pressure ranges, with modest process changes required for each.

High Volume: Throughput



- Good news: Fewer die variants –

  → "good" yield at die level

  → limited # of packages

  → well-defined operating conditions.

- Challenges:

  1st : Improving throughput:

  → Final assembly, test & trim <u>IS</u> the bottleneck.

  2nd : Reducing fall-out & handling issues / improving assembly yield.

- Examples of tests affecting throughput:
  - Testing over mechanical frequency – mechanical placement, settling time, hysteresis…
  - Testing over pressure – pressure source stabilization, eliminating leaks, hysteresis …
  - Testing over temperature – thermal lags, hysteresis…
  - Testing over time for reliability, burn-in.
  - Laser trimming for analog calibration & Package / die / sensor(s) tracking.

Outline

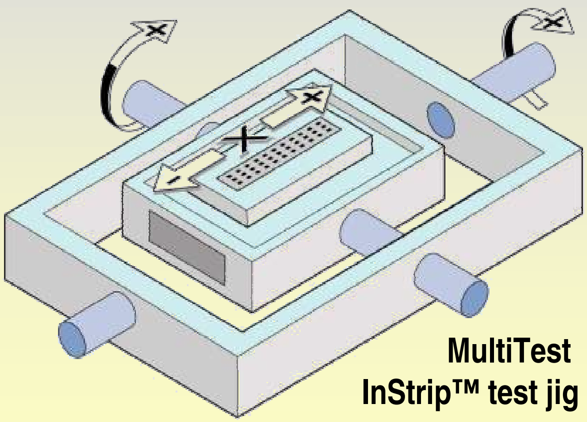
- Background.
- Motivation.
- Challenges facing the testing of packaged sensors:
  - During development.
  - In low-to-mid volumes.
  - For high volumes.
- Options available for testing sensors in high volumes.
- Trends in current approaches to testing in high volume.
- Conclusions and strategies going forward.

High-throughput Test Equipment

- Much still custom, e.g. Measurement Specialties, GE Sensing, Motorola/Freescale, Honeywell, Merit Medical, MEMSIC, etc.
  - Tests are often application specific, e.g. inkjet print heads, micromirrors…
  - Limited by lack of package standardization.
- Solution providers emerging:
  - MultiTest Electronic Systems
  - Unholtz-Dickie
  - Blue M (Lunaire)
  - SPEA
  - Mensor
  - Teradyne
  - National Instruments
- Consumer electronics volume for accelerometers, gyros, and IMU's is creating a market for test equipment suppliers.

Off-the-Shelf Volume Test Equipment

- Best systems *handle* 8,000 units per hour; gravity draw. *Test* is still slow.
- Some package standardization around DIL & SO.
- Multi-unit test parallelization, to obviate sensor mechanical time-constants.



MultiTest InStrip™ test jig

- Trends:
  - Leadless packages such as LGA, QFN, MFL attractive for CE miniaturization.
  - Smaller packages allow faster parallel testing.
    - Reduced thermal lag.
    - Reduced mass on shaker.
  - Smaller package electrical pads pose problem with reliable connectivity during test.
  - Multiple sensors in one package.

Outline

- Background.
- Motivation.
- Challenges facing the testing of packaged sensors:
  - During development.
  - In low-to-mid volumes.
  - For high volumes.
- Options available for testing sensors in high volumes.
- Trends in current approaches to testing in high volume.
- Conclusions and strategies going forward.

Approaches

- Goal: To reduce the burden of testing at final assembly.
- A mixture of approaches:
  - Moving back-end testing to the die-level, e.g. Wafer-Level Packaging (WLP) and testing.
  - Built-in Self-Test (BIST).
  - Higher performance sensor die.
  - Better assembly solutions.
  - Designing for Test (DFT).
  - *Virtualization of Test* ?

Wafer-Level Packaging (WLP)

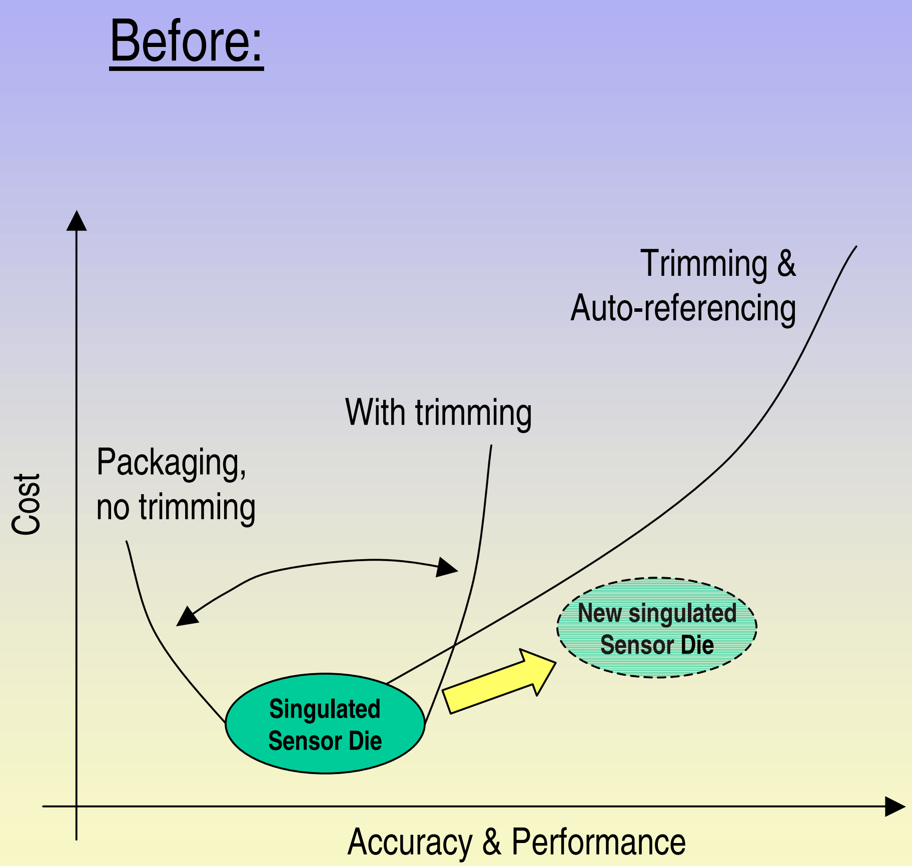
- Provides:
  - Electrical testing & emerging mechanical test methods at the wafer-level.
  - Higher-throughput testing of pressure, acceleration, temperature…
  - Mechanical integrity and stress control and repeatability.
  - Protection from contamination and robustness during wafer singulation.
- Possibilities:
  - WLP may allow many range of applications without stringent demands on sensor die performance.
- Challenges:
  - Ability to obviate test and trimming at final assembly for ideal performance still unclear.

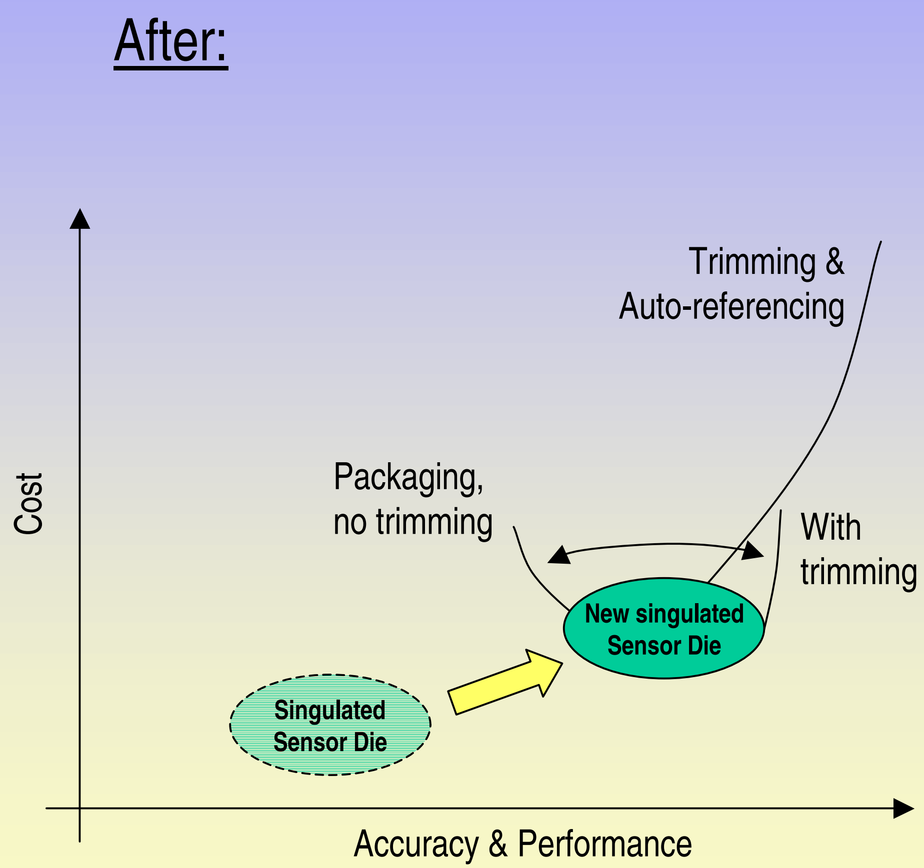
Built-In Self Test (BIST)

- Ideally suited for devices that can be electrostatically actuated.
- Process characterization: *In-situ* pull-in and resonance test structures (M-TEST) for mechanical property extraction & geometry characterization.
- Device characterization: Use electrical signals to simulate mechanical stimuli.
  - Analog Devices pioneered this concept with their ADXL-50 in 1990's.
- Approaches to apply this to pressure are in venture phase.

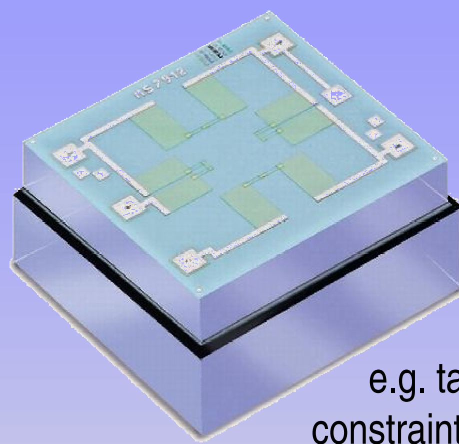
Higher Performance Sensor Die

Make a better die at higher cost, but reduced overall cost.





Solutions at the Die Level



e.g. tall constraints

- Stress-immunity:
  - → Allows more slop in assembly, keeping costs low, or
  - → Introduces package-level performance repeatability, reducing # of calibration test points.
- Possibilities:
  - – Cheaper assembly possible for low-performance applications.
  - – Tighter tolerances on material & geometry specifications allows greater flexibility to trim.
- Challenges:
  - – Obviating test & trim at final assembly for ideal performance still unclear.
- Alternatively:
  - – Remove off-chip analog trim by an "*All-digital*"™ calibration approach.

Solutions at Package / Assembly

- Designing into smaller, but robust packages that reduce test time per unit.
  - Reduced thermal lag.
  - Reduced mass on shaker, or more devices in parallel.
- Minimize packaging variations so that test equipment can be standardized – eliminating customization.
  - Design fewer packages but for larger ranges of operating conditions.
- Tighter control over assembly parameters.
  - Introduce automated visual inspection.

Designing for Test (DFT)

- Adding testability features at the die-level that allow assessment of the manufacturing process.
  - In-situ test structures.
  - Structures that help monitor extraneous environmental parameters that affect sensor performance.
  - Requires parameterization of variables affecting performance all the way through assembly.
- DFT establishes a framework over which designers, fabs, assemblers, and final testers can communicate during development and carry forward that information into high-volume to allow for process debugging, and streamline testing.

Virtualization of Test

- Details only emerging…
  - But a logical consequence of:
    1. Processes that are well-controlled and repeatable, and
    2. Input variables that are well-correlated to performance output.
  - Ideal for design flow where end users can easily input models into their own systems.
- … stay tuned ☺

Outline

- Background.
- Motivation.
- Challenges facing the testing of packaged sensors:
  - During development.
  - In low-to-mid volumes.
  - For high volumes.
- Options available for testing sensors in high volumes.
- Trends in current approaches to testing in high volume.
- Conclusions and strategies going forward.

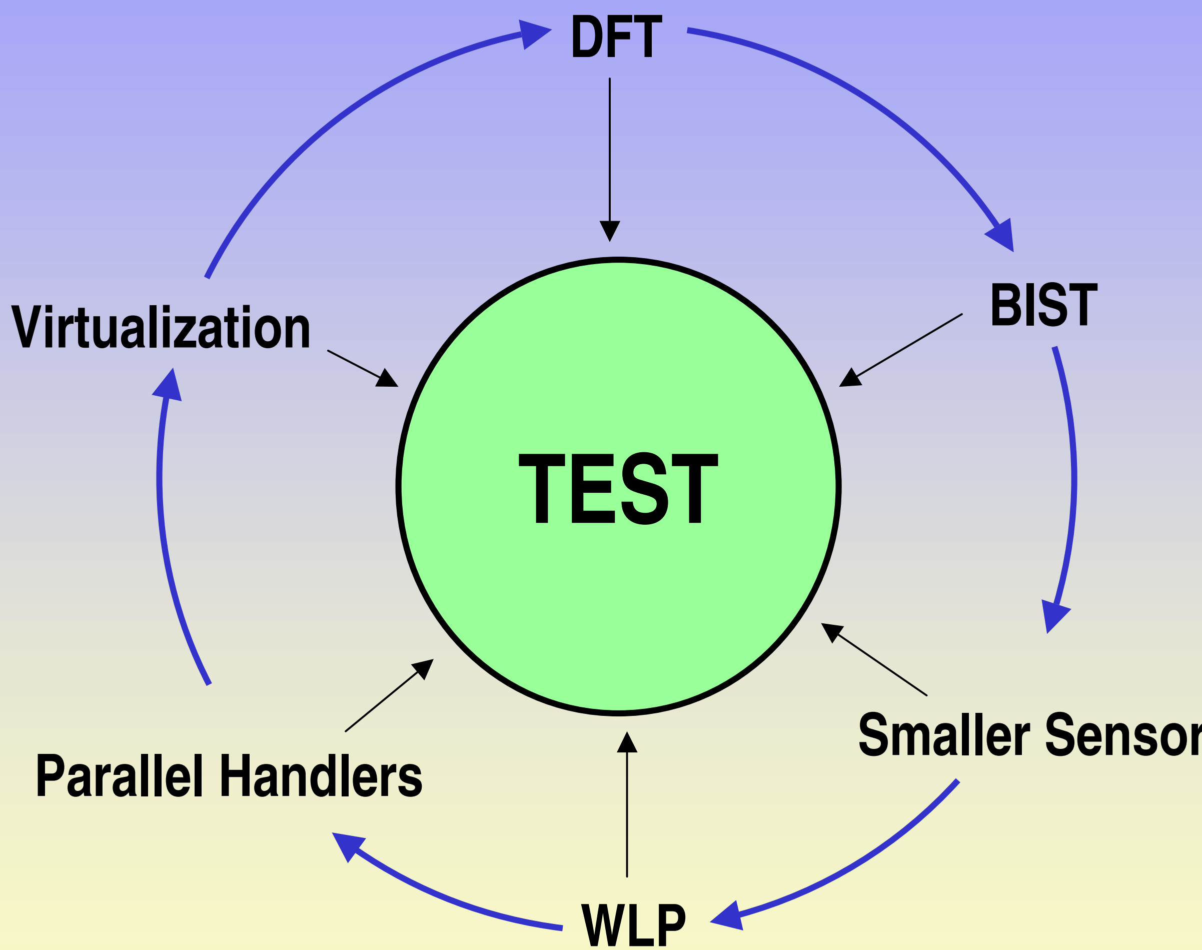
Areas in Continual Improvement

- Tighter control of assembly.
- Designs immune to packaging.
- Better feedback into design.
- Designing for test.
- Better automation for test.

Conclusions

- Requires savvy understanding of end application needs to affect full process of chip-to-assembly development and manufacturing.
  - Cannot plan on product pieces in isolation.
  - Program management highly critical.
- Cycle-time and cost would suggest one push as much backend into wafer-level as possible, so as to:
  - Reduce cost for testing & customization at package level.
  - Increase throughput.
  - Obviate difficulty and expense of diagnosing problems that happen at the packaging end resulting in band-aid solutions, re-work, or in the worst case, die redesign.

A Holistic Prospect for Test



Ultimate Vision

Because final test is and will be the minimum requirement to guarantee quality of the materials produced

…

The goal is to eliminate as many tests as possible to reduce the wafer start – to – customer delivery cycle-time.

Contact Information

Raj Gupta, Ph.D.

Owner, Volant Technologies

33 Vandewater Street, Ste 205

San Francisco, CA 94133

OFF: +1.415.391.0426

FAX: +1.425.675.6006

gupta –at– terahz –dot– org